Effects of bias cooling on charge states in heterostructures embedding self-assembled quantum dots

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Carrier transfer behavior has been investigated in selectively doped InGaAs/AlGaAs heterojunctions, in which a layer of self-assembled InAs quantum dots is embedded in close vicinity to a two-dimensional electron gas (2DEG). We applied the bias-cooling technique to derive information on the electron exchange properties from the bias dependence of the capacitance-voltage (CV) spectroscopy. Noise is observed in the CV results at large reverse biases after sufficiently negative bias cooling. The noise is temperature sensitive and can be eliminated when raising the temperature to 130 K. In combination with the experimental results in the control sample, we find that the noise induced by the bias cooling is most likely associated with the hot-electron trapping and detrapping in DX centers in the selectively doped AlGaAs layer. The effect of light illumination on the CV results supports our speculation on the noise origin. Furthermore, the variation in the 2DEG carrier concentration and mobility with bias-cooling processes has been discussed, which provides a direct insight into the vertical charge-transfer mechanism among the quantum dot related electronic states, DX centers, and 2DEG channel.

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I. INTRODUCTION

Considerable efforts have been expended in the study of self-assembled quantum dots (SAQDs), grown by the Stranski-Krastanov growth mode, because of their importance in fundamental physics and in device applications.[1–3] For the investigation of the internal electronic structure as well as the electron exchange dynamics between the dots and the neighboring environment, capacitance-voltage (CV) spectroscopy has proven to be a valuable tool. Recently, for a number of experiments it has been of interest to use a two-dimensional electron gas (2DEG) instead of a three-dimensional (3D) electron background as a reservoir to monitor the ac tunneling current between the dots [zero-dimensional (0D) system] and the two-dimensional (2D) system.[4–8] Measured changes in capacity are closely linked to the charging states of the coupled systems.

The bias-cooling technique has been used to study the dynamics of DX center occupation and charge transfer in heterostructures.[9–12] In this technique, a large negative bias is applied to the gate at a temperature higher than the DX center freezing temperature, which fully depletes any occupied donor centers. The bias is maintained until the sample is cooled to a temperature well below the freezing temperature, and then the static bias is removed. Electrons flood back into the region of the donors, but because of insufficient thermal energy for spontaneous lattice distortion the electrons will occupy only the shallow states around the donors and can be removed by subsequent application of the gate bias. The idea of this technique is to suppress the effect of DX centers due to the frozen energy states at low temperature. Moreover the usual approach is to use CV spectroscopy to characterize the 2DEG system by measuring the capacitance between the gate and 2DEG channel. The depletion of the 2DEG channel occurs by applying negative voltages on the gate and is characterized by a threshold voltage, below which capacitance becomes voltage independent and very close to zero. In recent years, an increasing number of optical and electrical experiments, such as photoluminescence and deep-level transient spectroscopy, have suggested the possibility that electronic deep levels might coexist with the quantum dots (QDs) around or in the dot layer.[13–18] As with the method to monitor the effect of DX centers, applying the bias-cooling technique to study the carrier transfer behavior among the electronic states in a heterostructure with embedded self-assembled QDs may give further understanding of the deep-level states coexisting with quantum confinement states and provide information about their effects on the 2DEG systems.

In this work, we apply the bias-cooling technique to study the CV spectroscopy of the InGaAs/AlGaAs heterostructure, in which InAs dots are embedded in the vicinity of the electronic channel. The data indicate the coexistence of deep levels with QDs. Surprisingly, at the same time, noise is observed in the CV curves at high reverse biases after bias cooling. The noise is temperature dependent and can be eliminated above 130 K. Over the last several decades the physical mechanisms behind the noise, especially the low-frequency noise in semiconductor devices, have been broadly investigated.[19–23] One of the common features in the experimental data reported in the literature proposes that noise is closely related to the charge traps in the structures. The existence of the noise in our control sample without QDs under the same bias-cooling conditions suggests that the observed noise may be associated with the DX centers localized in the δ-doped AlGaAs layer rather than the deep levels coexisting with the dots. Further measurements of noise dependence on the light illumination support our speculation of the noise origin. By examining the variation in the 2DEG carrier concentration and mobility under different

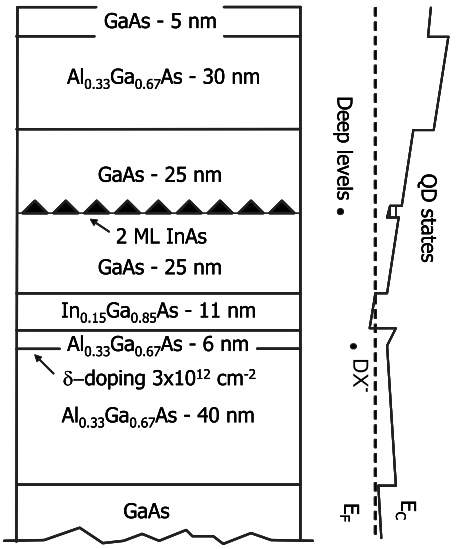

FIG. 1. Schematic illustration of the conduction-band diagram at the zero gate bias at room temperature and the growth structure of QD sample A. The QD sample has an inverted HEMT structure with InAs dots in the vicinity of the 2DEG channel.

bias-cooling conditions, we find that the 2DEG properties are closely linked to the charge states in the QD related electronic states and the DX centers in the selectively doped AlGaAs layer. Therefore, our work reports the direct observation of the noise generation and elimination in the CV spectroscopy using the bias-cooling technique. The understanding of the physical origins of the noise is essential for the formulation and interpretation of the underlying mechanisms in the devices. Studies of the noise may also provide a unique opportunity to obtain a detailed understanding of the electrically active traps in the structures.

II. EXPERIMENTAL DETAILS

Two QD samples (referred to as sample A and sample B, respectively) were grown by solid-source molecular-beam epitaxy (MBE) in our experiments. Both QD samples A and B consist of the same inverted high electron mobility transistor (HEMT) structure with a strained $In_{0.15}Ga_{0.85}As$ quantum well. Figure 1 shows schematically the structure and potential profile of sample A. Sample B has the same layer structure as sample A except that it has a thinner AlGaAs barrier (10 nm) between the gate and the QD layer. For the sake of comparison, a control sample was also grown under the same condition as that of sample A without the QD layer and the neighboring GaAs matrix. The formation of QDs with 2-ML InAs coverage was monitored *in situ* by reflection high-energy electron diffraction (RHEED), and the QD nucleation was observed via the change in the RHEED pattern from streaky (2D growth) to spotty (3D growth). The resulting quantum-dot density was around 3×10^9 cm^{-2}, as determined by imaging uncapped samples using an atomic force microscope. The photoluminescence properties as well as the more detailed characteristics of the HEMT structures have been reported elsewhere.[24,25] For the capacitance measurement, the ring-shaped ohmic contacts were fabricated by alloying Au-Ge-Ni/Au at 450 °C, while the square-shaped Schottky contacts with 1×1 mm^2 in width and length were defined by evaporating 30-nm Al on the surface in the middle of the ohmic contacts. In order to allow some light to transmit the gate, we have carefully controlled the thickness of the Al layer. Capacitance measurements were carried out using an Ametek signal recovery Model 7265 lock-in amplifier. Moreover current-voltage measurements were performed after each bias-cooling process by a Keithley 6430 dc source meter.

Hall-bar devices with a metallic top gate were also prepared in order to obtain the transport properties of the 2DEG channel under the different bias-cooling conditions. The mobility can be determined by the gate voltage dependence of the saturation drain current similar to the metal-oxide-semiconductor field-effect transistor (MOSFET) measurements in the saturation region.[26] Moreover the concentration can be calculated from the conductivity of the 2DEG. All the electrical measurements have been performed in dark in a He cryostat.

III. RESULTS AND DISCUSSION

In the following study, we first apply bias-cooling processes to investigate the CV characteristics of the QD samples. Noise is observed in the CV curves at large reverse biases after sufficiently negative bias cooling. Next, the temperature dependence of the noise is studied and shows that noise is temperature sensitive and can be eliminated when raising the temperature beyond 130 K (the DX center freezing temperature). Such coincidence suggests that the noise might be related to the DX centers in the selectively doped AlGaAs layer. The control sample without QDs is then examined. Moreover the existence of noise in the control sample rules out the possibility that noise originates form QDs and their coexisted deep levels. Further analysis suggests that the noise induced by the bias cooling is most likely associated with hot-electron trapping and detrapping in the DX centers. The effect of light illumination on the CV results, as well as the published reports, also supports our speculation on the noise origin. Finally, we study the variation in the 2DEG carrier concentration and mobility under different bias-cooling processes, which can provide direct information of charge transfer among the QD related electronic states, the DX centers, and the 2DEG channel.

The bias-cooling processes were performed on sample A from room temperature to 50 K under fixed negative gate voltages V_g ranging from 0 to −3 V. The gate bias was maintained until 50 K, which is well below the DX center freezing temperature (about 130 K).[27] Then the bias was removed and the CV measurement was performed at a low frequency of 80 Hz and a small-signal ac voltage of 10 mV. Figure 2 depicts the capacitance traces after bias cooling at different voltages. At a reverse bias $V_r > -1.5$ V, the 2DEG channel is charged with electrons and becomes the active back electrode once its conductivity is sufficiently high. The measured capacitance is therefore constant and agrees well with the value of 1.22 nF, which is estimated from the dis-

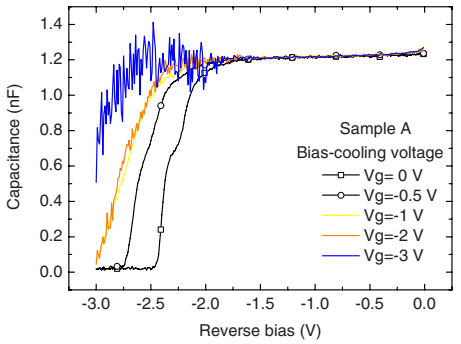

FIG. 2. (Color online) CV characteristics of sample A after bias-cooling processes at different gate voltages V_g ranging from 0 to −3 V. The shift of the threshold voltage reflects the changes in the carrier concentration in the 2DEG.

tance between the 2DEG and the gate. The capacitance curve shows a steep and dramatic decrease due to the depletion of the 2DEG channel at threshold voltage V_T. As shown in Fig. 2, V_T moves to more negative voltages with increasing negative bias-cooling voltage from 0 to −3 V indicating the existence of more charges in the system (mainly the 2DEG) after bias cooling.

Two possible sources, resulting in more charges in the 2DEG channel after bias cooling, are the deep levels coexisting in the dot layer and the DX centers in the modulation-doped AlGaAs layer. We exclude the contribution from the QD intrinsic states because, as shown by the conduction-band profile in Fig. 1, the states lie well above the Fermi level E_F at zero gate bias. In the bias-cooling process, only negative cooling voltage is required to discharge the electronic states in the structure in order to suppress their effect on the CV characteristics at low temperature. This leads to empty QD states during the bias-cooling operation. In the bias-cooling experiments, when the cooling bias V_g changes from 0 to −2 V, the threshold shift can be explained by the discharging of the occupied deep levels in the dot layer as their energy states are raised beyond the bulk Fermi level by the gate voltage. This gives rise to more free electrons and consequently the depletion occurs at a more negative voltage. The conduction-band profiles during bias cooling at different cooling voltages can be illustrated as Fig. 3. The conduction-band profiles as a function of depth were calculated by a Green's-functions simulator called WINGREEN.[24] The coexistence of the deep levels with QDs has been shown and the corresponding memory effect due to the deep levels has been reported as well in our previous work.[18,24,25] The overlap of the CV curves at $V_g=-1$ and −2 V rules out the contribution of the DX centers when $V_g>-2$ V and suggests that the deep levels localized in the dot layer have been all raised above the bulk Fermi level and completely discharged. Since the DX centers in the δ-doped AlGaAs layer are screened by the 2DEG channel, the contribution of the DX center occurs only after bias cooling when $V_g<-2$ V, leading to a further threshold shift after bias cooling with a negative gate voltage of −3 V. Surprisingly, noise appears in the CV curves at the large reverse biases after the bias-cooling processes with $V_g=-2$ and −3 V. Since the low-frequency noise observed in semiconductor devices is purportedly caused by individual traps in the structures,[19] the noise obtained after bias cooling with large negative gate voltages might be associated with the DX centers, which will be further confirmed by the later experimental results. There is an apparent step at around $V_r=-2.3$ V in the CV trace after normal bias cooling ($V_g=0$ V). The reason for this is not clear, but it may be related to the carrier accumulation at the interface between the AlGaAs layer and GaAs background where the measured capacitance is in agreement with the estimated value from the distance between the gate and the interface.

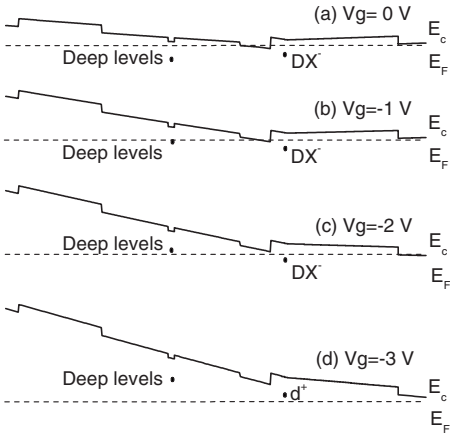

FIG. 3. Conduction-band profiles of QD sample A during bias cooling at (a) $V_g=0$, (b) −1, (c) −2, and (d) −3 V. For clarity, the QD states are not shown in the figure. At the bias-cooling voltage of −3 V, DX centers in the selectively doped AlGaAs layer are lifted above the bulk Fermi level, which discharges the negative charge DX^- centers to form the positive charge d^+ states.

To identify the nature of the noise observed in the CV curve after bias cooling with $V_g=-3$ V, noise dependence on the temperature was measured and the results are shown in Fig. 4. Sample A was biased at $V_g=-3$ V and cooled down to 50 K. The noise was observed at the large reverse biases in the CV curve, referred to as the "50 K" curve in Fig. 4. Under the normal bias condition ($V_g=0$ V) the temperature was then raised to 90 K and maintained for 15 min and then cooled down to 50 K to measure the capacitance,

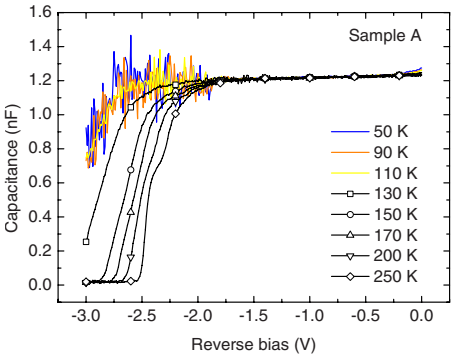

FIG. 4. (Color online) Temperature dependence of the noise generated by the bias-cooling process at $V_g=-3$ V. The noise is temperature dependent and can be eliminated when raising the temperature above 130 K.

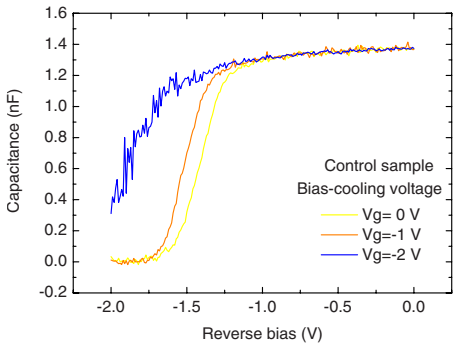

FIG. 5. (Color online) CV characteristics of the control sample after bias-cooling processes at different gate voltages V_g ranging from 0 to −2 V.

which generated the so-called "90 K" curve in Fig. 4. Using the same method, we studied the effect of the temperature ranging from 90 to 250 K. The noise can be eliminated when raising the temperature higher than 130 K. In the modulation-doped AlGaAs heterostructures, Si doping produces different deep donor centers (DX centers) into the $Al_xGa_{1-x}As$ layer and the DX center freezing temperature depends on the Al mole fraction x.[12,27] The freezing temperature of the DX centers in $Al_{0.33}Ga_{0.67}As$ layer has been proposed to be 130 K. The coincidence of the noise elimination temperature with the DX center freezing temperature thus indicates that the noise might be related to DX centers.

To rule out the noise originating from the QDs and the coexisting deep levels, we performed the bias-cooling measurement on the control sample without the dot layer and the neighboring GaAs matrix, shown as Fig. 5. The noise also exists in the CV curve after the bias-cooling process with $V_g=-2$ V. Because of the smaller distance from the 2DEG channel to the gate, the depletion of the 2DEG channel occurs at smaller reverse biases and the noise generation occurs at relatively smaller negative cooling bias of $V_g=-2$ V. The threshold shift is smaller than that in the QD sample because of the absence of the effect of the deep levels coexisting with QDs. Such data, therefore, rule out the possibility of the noise being related to the dots and suggest that it might be associated with the DX centers.

DX centers are the intrinsic states of the isolated donor atoms in III-V semiconductors and their alloys.[28] It is now widely accepted that DX levels in n-typed $Al_xGa_{1-x}As$ are ground states of isolated donors in distorted configurations, which are stabilized by trapping two electrons. The leading microscopic model is that the distortion occurs when group IV donor, substituted on group III lattice site, moves along a ⟨111⟩ axis toward an interstitial site, which is characterized by a negative effective Hubbard correlation energy (negative U). Based on the negative U nature, the lattice-relaxation model shows that thermal capture and emission of electrons in the DX centers occur via an intermediate state,[29] which requires sufficient thermal energy to overcome the barrier. Thus, one of the most striking properties of the DX centers is that both emission and capture of electrons are thermally activated, with unobservably small rates below a critical temperature.[27] This temperature is referred to as the DX center freezing temperature, below which the energy states are frozen in and the capture and emission rates are negligible. Also, the model indicates that donors are bistable, existing either in substitutional configurations having shallow hydrogenic ground states (neutral d^0 or positive charge d^+ states) or in distorted configurations with DX centers as ground states [negative (two-electron) DX^- or neutral (one-electron) charge DX^0 states]. Whether DX configurations are stable or metastable states depends on the alloy compositions.[28] With $x=0.33$, the DX levels in our n-typed $Al_{0.33}Ga_{0.67}As$ are stable states. In thermal equilibrium the occupation of the DX centers is determined by their energy position relative to that of the Fermi energy in the given sample. Therefore, the donor Si atom in our structures exists either in a positively charge d^+ state or as negatively charge DX^- centers. Correlations established between these two sets of charge states can be modulated by the bias-cooling technique as shown in Fig. 3.

In order to clarify the mechanism of noise generation, we further analyze the effects of bias cooling on the charge-state variation in the DX centers in the QD sample. At room temperature and zero bias, DX centers are occupied by two electrons in thermal equilibrium. After normal bias-cooling process ($V_g=0$ V), as shown in Fig. 3(a), they are frozen in as the negatively charge states at low temperature. Under the bias-cooling conditions at $V_g=-1$ and −2 V, as shown in Figs. 3(b) and 3(c), DX centers are also negative charged since they are below the bulk Fermi level. Figure 3(d), however, shows that cooling at a gate voltage of −3 V on the QD sample from room temperature depletes any occupied donor centers fully since they are lifted well above the Fermi level. Electrons release from the negative charge DX^- states forming the positive charge d^+ states.[29] In the bias-cooling process, this bias is maintained down to a temperature of 50 K, well below the DX center freezing temperature of 130 K in our structures, and then the bias is removed. Due to the lack of sufficient thermal energy for spontaneous lattice distortion to occur, the electrons can occupy only the shallow states around the donors and will be removed by the subsequent application of gate bias. Therefore, the distribution of donors shown in Fig. 3(d) is frozen into the sample at low temperature. The DX levels remain empty and become metastable. This leads to more free electrons in the 2DEG channel and the shift of the threshold voltage toward a more negative voltage.

At the same time, during the CV measurement the large reverse bias induces the high electric field in the structure. Figures 6(a) and 6(b) present the conduction-band profiles at a reverse bias of −3 V applied to QD sample A cooled without bias and with $V_g=-3$ V, respectively. The electric field with positive charge d^+ states at the selectively doped AlGaAs layer is rather higher than that with negative charge DX^- centers according to Poisson's equation,[26] which can cause hot-electron trapping in the DX centers.[30,31] Such a capture process is expected from the large lattice-relaxation model since a hot electron entering the resonant state can trigger the lattice relaxation without the assistance of thermal phonons. Due to the DX levels well above the bulk Fermi level and the effect of the strong electric field, the trapped charges might be released after a random delay. This random capture and release of carriers by the DX centers under the

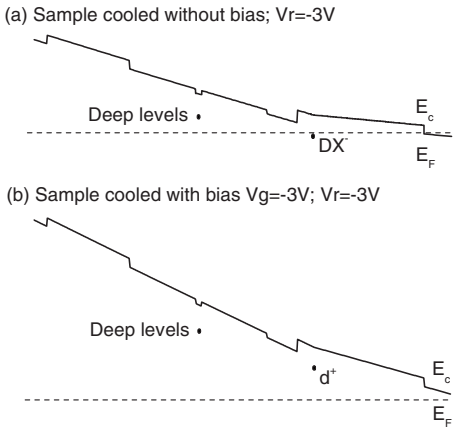

FIG. 6. Conduction-band profiles for a reverse bias $V_r=-3$ V applied to QD sample A after bias cooling at (a) $V_g=0$ and (b) −3 V.

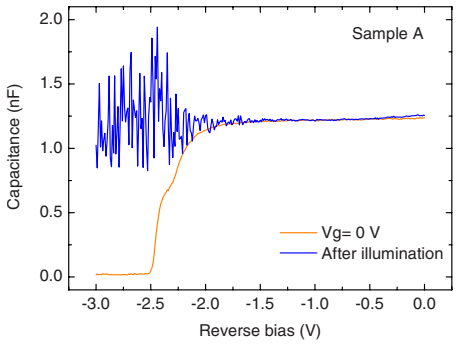

FIG. 7. (Color online) Effect of light illumination on the CV characteristics of sample A after normal bias cooling. The CV measurement was performed in dark after exposure of the sample to visible light at 50 K, which gives rise to the curve referred to as after illumination. For the purpose of comparison, the CV curve at 50 K after normal bias cooling without light illumination is also included in the figure.

high electric field induce random current in the structures superposing on the output signal, which is responsible for the noise observed in the CV curves after the bias-cooling process in Fig. 2. A close look at Fig. 2 reveals that the noise level is rather related to the cooling voltage than to the applied reverse bias since it seems to be independent of reverse bias once it is switched on. There might be two factors affecting the noise level here. One is the hot electrons whose energy and concentration are dependent on the applied reverse bias, while the other is the density of DX centers, which have been lifted above the Fermi level to form the positive charge states during the bias-cooling process. The independence of noise level on the reverse bias suggests that the density of the positive charge d^+ states might be the limiting factor. Further experiments are required to clarify the underlying mechanism. During the temperature-dependent measurements, when the temperature increases above the DX center freezing temperature of 130 K, the DX centers can be thermally activated and electrons can flow back into the DX centers. Such negative charge states become frozen at the low temperature of 50 K, which corresponds to the threshold shift toward low negative voltage due to reduced electron concentration in 2DEG channel and the absence of noise in the CV characteristics as shown in Fig. 4. When the temperature is high enough to activate all the DX centers, the CV curve observed at 50 K becomes the same as that obtained under the normal bias-cooling condition from the room temperature, such as the "250 K" curve in Fig. 4.

The previous work by Longoni *et al.*[23] dealt with the study of the "trapping noise" that was the low-frequency noise caused by the random capture and release of carriers by localized traps. The trapping noise was believed to give rise to the random telegraph signal in the semiconductor devices. The hot-electron capture by DX centers has also been related to the device instability in some other reports.[30–33] Theis *et al.*[30] studied the hot-electron trapping by DX centers by recording conductance transients in short channel modulation-doped field-effect transistors. Kunets *et al.*[33] found that the higher electric fields in the device active area could cause additional generation-recombination noise due to hot-electron trapping and applied the deep-level noise spectroscopy to show that the noise came from the DX centers in the AlGaAs barrier. These observations support our explanation of the noise generated by the bias-cooling technique. Recently, switching noise in GaAs/$Al_xGa_{1-x}As$ lateral gated devices has been investigated by monitoring the conductance fluctuations by Pioro-Ladrière *et al.*[34] They found that cooling with a positive bias on the gates reduced the density of ionized donors by freezing free carriers into DX centers in the doping layer and thus dramatically reduced the noise. This is in agreement with our observations. A model that localized states near the active region of the device captured electrons from the leakage current tunneling through the Schottky barrier was proposed to explain the origin of the switching noise. Direct evidence of the leakage current was provided by monitoring the charge trapped in a closed quantum dot. In our experiments, the current-voltage measurement was performed between the gate and the 2DEG channel after each bias-cooling process. Only a slight increase in the leakage current was observed after bias cooling with large negative cooling voltages that led to pronounced noise in the CV curves (not shown here). Because of lack of direct evidence correlating the generated noise with the leakage current, such as in Ref. 34, it is difficult to conclude whether the noise induced by the bias cooling comes from an increase in gate leakage. Further experimental and theoretical investigations are required to clarify the relation between the noise and the gate leakage current.

Moreover, the persistent photoconductivity (PPC) effect is perhaps the most characteristic phenomenon related to DX centers.[35] According to their lattice-relaxation model, if the sample is illuminated with visible light, which transfers the electrons from the DX centers to the conduction band, the increased free-electron concentration persists at low temperature after the light is switched off. Figure 7 presents the effect of illumination on the CV characteristics. QD sample A was cooled down to 50 K under the normal bias-cooling condition of $V_g=0$ V, and the CV curve was recorded as a reference in Fig. 7. Then the sample was illuminated with white light for 10 min and the CV measurement was performed after the light was switched off, which corresponds to

the curve named as "after illumination" in Fig. 7. Noise exists at the large reverse biases, which is similar to that obtained after the bias-cooling process with $V_g=-3$ V. The noise is still observable after a long time interval. The persistence of noise might be the same as the PPC effect in nature as the occupied DX centers are completely discharged by the light and the electrons cannot move back into the DX levels at low temperature due to the large capture energy barrier. The capture process occurs because the high electric field causes the hot-electron trapping, which generates the noise. Such effect of light illumination on the CV characteristics thus supports that the noise originates from the hot-electron trapping/detrapping in the DX centers in the selectively doped AlGaAs layer.

Having identified the correlation between the deep-level states, including both deep levels coexisted with QDs and the DX centers in the selectively doped AlGaAs layer, and the noise in the CV characteristics, it is important to gain further insight into their effect on the transport properties of the 2DEG channel, which may allow improvement and optimization of the performance of the quantum devices based on III-V materials. Capture and emission of electrons in the deep-level states affect the carrier concentration, that is, the conduction in the electronic channel. In particular, changes in charge states of the DX centers in the region close to the InGaAs/AlGaAs interface will cause a local fluctuation in the density and Coulombic scattering of electrons in the 2DEG.[36,37] In order to quantitatively study these effects, bias-cooling technique was applied to investigate the variation in the 2DEG mobility and carrier concentration with different bias-cooling processes. Because of the limitation of the He cryostat where bias-cooling measurement was performed, we determined the electron density and mobility in the 2DEG channel using the following method. Source-drain current as a function of the gate voltage was measured on the Hall-bar devices after bias cooling. By plotting the square root of the drain current versus gate voltage, the field-effect mobility was determined in the saturation regime after fitting the data to extract the slope of the plot.[26] And then the carrier density was calculated from the conductivity of the 2DEG. In realistic device measurements, it is more usual to apply such a method to determine the carrier transport properties in semiconductor thin-film transistors than in a 2DEG system.[38,39] Thus error bars are given in the calculation results according to such indirect method. As shown in Fig. 8, the variation in a value determined from the source-drain current as a function of the gate voltage is less than 10%.

Figure 8 shows the 2DEG mobility and carrier concentration as a function of the cooling bias for the QD sample (sample B) and the control sample. Both samples have similar noise characteristics observed in the CV curves after the bias-cooling processes. In Fig. 8, the low-temperature mobility in the InGaAs quantum well looks much lower than those commonly observed in AlGaAs/GaAs 2DEGs. This might be due to the strong effect of the ionized donors, which are located in a very close vicinity (6 nm) of the 2DEG, and the effects of the alloy-disorder and intersubband scatterings, which have a strong influence on the mobility at high electron concentrations. The dominant scattering mechanism in our 2DEG will be discussed in detail later. Here, since we are

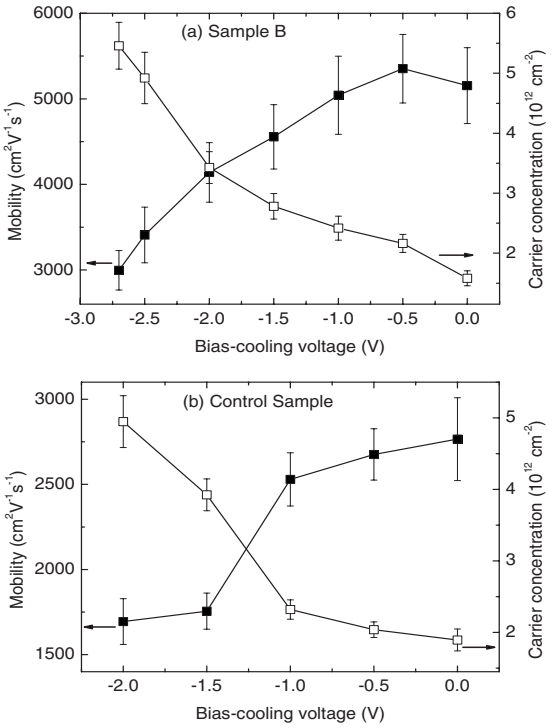

FIG. 8. Dependence of the 2DEG mobility and carrier concentration on the bias-cooling voltage at 50 K in (a) the QD sample (sample B) and (b) the control sample.

mainly interested in the changes in the mobility as a function of the cooling bias, we did not try to work out how each factor would contribute to the mobility measurements. Figure 8(a) shows that in the QD sample, the 2DEG concentration gradually increases with increasing negative bias-cooling voltage due to the bias-cooling induced carrier contributions from the coexisting deep levels when 0 V $>V_g>-2$ V and then from the DX centers beyond −2 V. However, the mobility decreases as the concentration increases.

It is of great importance to clarify the underlying scattering mechanism that limits the 2DEG mobility. At low temperature, such as 50 K in our measurements, phonon scattering is negligible and the scattering mechanisms limiting the mobility are ionized-impurity, alloy-disorder, or interface-roughness scatterings.[40] In general, ionized-impurity scattering can be due both to remote impurities from ionized donors in the δ-doped AlGaAs layer and to background ionized impurities present both in the well and in the barriers. The ionized-impurity scattering-determined mobility is a function of the density of the 2DEG, n_{2D}, and follows that $\mu \propto n_{2D}^{3/2}$.[40] And for the interface-roughness scattering, under the condition of $k_F\Lambda>1$, backscattering is reduced and the mobility increases with increasing electron density.[41–43] Here, k_F is the Fermi wave number, which can be estimated from the carrier concentration as about 10^8 m^{-1}. Moreover Λ is the coherent length of the interface, which is about 1 μm for the MBE-grown interface. So the above condition is easy to achieve in our samples. From the results in Fig. 8(a), we can therefore rule out ionized-impurity and interface-roughness scatterings as a limiting scattering mechanism in our 2DEG.

The theoretical calculation in an $In_{1-x}Ga_xAs$ quantum well indicated that the mobility was inversely proportional to the density for alloy-disorder scattering and for $n_{2D} > 5 \times 10^{11}$ cm^{-2} alloy-disorder scattering was probably the dominant scattering mechanism.[42,44] This may explain our observation in Fig. 8(a) that the mobility drops with the increment of the density. Another possible reason might be due to the carrier scattering between the ground subband and the first excited subband as the increasing carriers probably occupy the first excited subband.[45]

In the control sample, the correlation between the 2DEG mobility and concentration is similar to that in the QD sample. However, the changes in the electron concentration and mobility are relatively small at $-1\ \text{V} < V_g < 0\ \text{V}$ before the contribution of the DX centers occurs due to the absence of the coexisting deep levels. For $V_g < -1\ \text{V}$, the increase in the concentration and the decrease in the mobility are apparent, which can be accounted for by the modulation of the DX centers after the bias-cooling processes with the large negative cooling voltage.

In realistic device applications, the quantum-dot states in the conduction band are usually filled with electrons either by optical or electrical means. The coexistence of deep levels with QDs might affect the carrier exchange between the QD intrinsic states and the neighboring environment.[18] According to the discussions above, applying bias cooling at a voltage of $V_g = -2\ \text{V}$ on QD sample A depletes occupied deep-level states in the dot layer. Such empty states are frozen in at low temperature, leading to more electrons in the system and consequently the threshold voltage moving to a more negative value, as shown in Fig. 2. This finding opens the possibility to populate the quantum-dot intrinsic states by the gate bias at low temperature without refilling the coexisting deep levels by the bias-cooling technique. A potential advantage is that we could exclusively study the QD intrinsic states by suppressing the effect of the coexisting deep levels. For optical experiments, however, the gate used to apply bias on the structure usually masks the laser. Transparent or semitransparent gate, such as a thin metal layer, is required for bias-cooling processes. The charge state in deep levels could be modulated by the bias-cooling technique, and their effects on the QD photon excitation properties could be experimentally investigated. Noise would not be an issue under these conditions since it is related to DX centers rather than QDs and their associated deep levels. Consequently, further studies using bias-cooling technique could not only provide important insight into the physical correlation between QD intrinsic states and the coexisting deep levels but also lead to important implications in optimization of the performance of QD-based electronic and optical devices.

IV. CONCLUSION

The bias-cooling technique has been applied to study the charge-state variation in the InGaAs/AlGaAs heterostructures with embedded self-assembled QDs. The coexistence of deep levels with QDs has been further evidenced by the bias dependence of the CV spectroscopy. The noise in the CV characteristics was studied by the bias-cooling technique. We have demonstrated that the noise can be generated by the bias-cooling process and eliminated by raising the temperature above 130 K, which is about the freezing temperature of the DX centers. Combining the experimental results of the control sample we point out that the noise is associated with the DX centers in the δ-doped AlGaAs layer rather than due to quantum dots. The effect of light illumination on the noise also indicates that the noise is caused by the high electric field due to the hot-electron capture and emission from the DX centers. Furthermore, the properties of carrier transfer among the deep levels coexisting with QDs, the 2DEG channel and the DX centers have been studied under the bias-cooling conditions. It is found that whereas the 2DEG carrier concentration increases with the increase in the bias-cooling gate voltage, the mobility significantly decreases. Possible mechanisms have been discussed.

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